In The Claims:

Please amend the claims according to the following listing of claims and substitute it for

all prior versions and listings of claims in the application.

1-2. (cancelled)

3. (currently amended) A microcontroller device for extending memory address space by

inserting a waiting state, wherein the device is coupled to an external memory through a bus, and

the external memory has stored at least a first program, the device comprising:

a read-only memory (ROM), for storing a second program;

a central processing unit (CPU), coupled to the ROM, for executing the first program or

the second program; and

a memory interface controller, for inserting a waiting state into the CPU when the CPU

intends to execute an instruction of the first program stored in the external memory; ┬

The device of claim 1, wherein the memory interface controller comprises:

a memory interface, coupled the bus, serving as a transmission interface between the

memory interface controller and the bus;

a range checking unit, used to judge whether or not an address of an information, which is

to be accessed by the CPU, is located within a predetermined range, and selectively issuing a

range checking signal; and

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a state control unit, coupled to the memory interface, the range checking unit, and the CPU, used for inserting the waiting state into the CPU when the range checking signal is received.

4. (cancelled)

5. (currently amended) A microcontroller device for extending memory address by inserting a waiting state, wherein the device is coupled to an external memory through a bus, and the external memory has stored at least a first program, the device comprising:

a read-only memory (ROM), for storing a second program:

a central processing unit (CPU), coupled to the ROM, for executing the first program or the second program: and

a memory interface controller, for inserting a waiting state into the CPU when the CPU intends to execute an instruction of the first program stored in the external memory, wherein the memory interface controller comprises:

a memory interface, coupled the bus, serving as a transmission interface between the memory interface controller and the bus:

a range checking unit, used to judge whether or not an address of an information, which is to be accessed by the CPU, is located within a predetermined range, and selectively issuing a range checking signal:

a state control unit, coupled to the memory interface, the range checking unit, and the CPU, used for inserting the waiting state into the CPU when the range checking signal is

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received; ~~The device of claims 3,~~ wherein the device further comprising an inquiry mode, and

the memory interface controller further comprising:

a buffer, coupled to the memory interface, for temporarily store the information accessed

from the external memory through the bus; and

a ready flag, coupled to the buffer and the CPU, wherein the CPU inquires the ready flag ,

and the CPU correctly accesses the information through the buffer when buffer has correctly

accessed the information of the external memory through the memory interface.

6. (original) The device of claim 5, wherein when the CPU sets the device to the inquiry

mode, the state control unit does not insert the waiting state into the CPU, and memory interface

controller is activated by executing a read memory instruction.

7. (original) The device of claim 5, wherein the buffer includes a plurality of registers, the

registers can store at least one byte information set.

8. (original) The device of claim 5, wherein the accessed information by the inquiry mode

includes voice information or music information.

9. (currently amended) The device of claim ~~1~~ 5, wherein a transmission unit in one time is

one bit, two bits, one nibble, or one byte.

10-12. (cancelled)

13. (currently Amended) An operation method on a microcontroller device for extending

memory address by inserting a waiting state, wherein the device at least includes a central

processing unit (CPU), the operation method comprising:

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setting a predetermined address range;

judging whether or not an address of a program instruction to be fetched is located within the predetermined address range;

inserting a waiting state into the CPU when the address is located out of the predetermined address range, until the program instruction is completely fetched; and

executing the program instruction by the CPU~~The operation method of claim 11~~, wherein the waiting state being inserted into the CPU cause a clock state of the CPU to remain.

14. (cancelled) .

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